Partition-based Task Mapping for Communication Energy Minimization in 3D Network-on-Chip

Sanghoon Kwak(kwak.sanghoon@gmail.com)
Intel Deutschalnd GmbH

Abstract

Abstract—Network-on-Chip designs have experienced a rapid development during the last decade and is a becoming a de-facto technique for communication among cores. 3D integration using Through-Silicon-Via (TSV) has received much attention recently as an alternative solution to overcome the bottleneck of wiring. Integrating 3D TSVs with the conventional 2D NoC takes full advantage of the characteristics TSV such as lower power consumption and much smaller delay. In this paper, an efficient task mapping algorithm to target reducing communication energy of 3D NoC, in which the procedure is decomposed into balanced min K-way partitioning algorithm and a heuristic partition arrangement to 2D plane. Experimental results demonstrate the proposed algorithm much less communication energy than the previous approaches.

For high-performance applicatoins such as 5G baseband modem, the requirement of HW throughput is extremly high. To meet this performance requirements, the baseband modems are split into number of subblocks and those subblocks should be efficiently connected in terms of latency, throughput, and power consumption.

Keywords: *Network-on-Chip, SoC, Through-Silicon-Via, Partitioning, Task Mapping, Low Energy*

Biography

Sanghoon Kwak received his PhD from the Dept. of Info. & Comm, GIST in 2009. He held post-doctoral research positions at the Dept of CS, University of Bristol and the Verimag Lab, Université Grenoble Alpes. He is working as digital design engineer in iCDG, Intel Deutschland GmbH, Germany, since Aug. 2017. His current research interests include network-on-chip architecture, hardware acceleration of deep-neural network, and design of 5G baseband modem, etc.