# Millimeter-scale computers as the next generation computing class for Internet-of-Everything

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**Abstract**

From mainframes in the 1950s to workstations in the 1960s, personal computers in the 1980s, laptops in the 1990s and now the current smartphones, one of the most evident trends in the history of computers is the increasing convenience and frequency of access by humans [1]. The miniaturization of the computer is an important factor in this trend, lowering cost, reducing the required space and providing mobility. The extrapolation of this trend indicates the birth of a new computer which is smaller, cheaper and more numerous than smartphones. The next generation computer will improve proximity to the object, the source of information, rather than to humans to allow much more aggressive miniaturization while improving the data quality. Thus, machine service for humans is expected to improve extensively through the emerging prevalence of miniaturized computers.

The most evident challenge is the ultra-low power consumption required by the small form factor. For example, a millimeter-scale Li thin-film battery provides nearly one-millionth of the energy capacity of an alkaline AA battery. Therefore, the circuit design regime must be switched from milliwatt to nanowatt level to support an equivalent system lifetime. Conventionally, the strongest driving force for such a hardware innovation has been process scaling, which has increased speed and the degree of integration while reducing power consumption. However, it has almost reached the limits of fundamental physical and economic barriers. Furthermore, such deep sub-micron technologies do not fit well on mm-scale computing platforms because their high leakage causes significant power penalties and analog-inaccuracy in the nanowatt design regime. Therefore, in the birth of the new computing platform of millimeter-scale sensor nodes, advances in circuit-level techniques will be the main driving force.

This talk based on recent publications introduces ultra-low power timing solutions [2-4], sensor interfaces [5-6] and communication circuits [7-9], that are key building blocks of miniaturized sensor systems.

[1] G. Bell, "Bell's Law for the Birth and Death of Computer Classes: A theory of the Computer's Evolution," in IEEE Solid-State Circuits Society Newsletter, vol. 13, no. 4, pp. 8-19, Fall 2008.

[2] T. Jang, M. Choi, S. Jeong, S. Bang, D. Sylvester and D. Blaauw, "5.8 A 4.7nW 13.8ppm/°C self-biased wakeup timer using a switched-resistor scheme," 2016 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, 2016, pp. 102-103.

[3] J. Lim et al., "A 224 PW 260 PPM/°C Gate-Leakage-Based Timer for Ultra-Low Power Sensor Nodes with Second-Order Temperature Dependency Cancellation," 2018 IEEE Symposium on VLSI Circuits, Honolulu, HI, 2018, pp. 117-118.

[4] Y. Zeng, T. Jang, Q. Dong, M. Saligane, D. Sylvester and D. Blaauw, "A 1.7nW PLL-assisted current injected 32KHz crystal oscillator for IoT," 2017 Symposium on VLSI Circuits, Kyoto, 2017, pp. C68-C69.

[5] S. Jeong et al., "Always-On 12-nW Acoustic Sensing and Object Recognition Microsystem for Unattended Ground Sensor Nodes," in IEEE Journal of Solid-State Circuits, vol. 53, no. 1, pp. 261-274, Jan. 2018.

[6] T. Jang et al., "A Noise-Efficient Neural Recording Amplifier Using Discrete-Time Parametric Amplification," in IEEE Solid-State Circuits Letters, vol. 1, no. 11, pp. 203-206, Nov. 2018.

[7] Wootaek Lim, Taekwang Jang, Inhee Lee, Hun-Seok Kim, D. Sylvester and D. Blaauw, "A 380pW dual mode optical wake-up receiver with ambient noise cancellation," 2016 IEEE Symposium on VLSI Circuits (VLSI-Circuits), Honolulu, HI, 2016, pp. 1-2.

[8] M. Choi, T. Jang, J. Jeong, S. Jeong, D. Blaauw and D. Sylvester, "A Resonant Current-Mode Wireless Power Receiver and Battery Charger With −32 dBm Sensitivity for Implantable Systems," in IEEE Journal of Solid-State Circuits, vol. 51, no. 12, pp. 2880-2892, Dec. 2016.

[9] T. Jang, S. Jeong, D. Jeon, K. D. Choo, D. Sylvester and D. Blaauw, "A Noise Reconfigurable All-Digital Phase-Locked Loop Using a Switched Capacitor-Based Frequency-Locked Loop and a Noise Detector," in IEEE Journal of Solid-State Circuits, vol. 53, no. 1, pp. 50-65, Jan. 2018.

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**Biography**

Taekwang Jang is currently an Assistant Professor at the Institute for Integrated Systems at the ETH Zürich, Switzerland. He received his B.S. and M.S. in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejon, Korea, in 2006 and 2008, respectively. From 2008 to 2013, he worked at Samsung Electronics Company Ltd., Yongin, Korea, focusing on mixed-signal circuit design including analog and all-digital phase-locked loops for communication systems and mobile proc