SiC manufacturing technology for sensors and lateral power transistors towards integrated circuits

Tobias Erlbacher(tobias.erlbacher@iisb.fraunhofer.de)
Fraunhofer Institute for Integrated Systems and Device Technology IISB

Abstract

The development of silicon CMOS technology in the 1960 has enabled a vast amount of innovative applications starting from mathematical computations over personal computing, infotainment and fast electronic control circuity to high-speed communication and integrated power solutions. The application temperature of silicon circuits in these applications is limited, however, to approximately 125°C. Fabrication technologies for temperatures up to 250°C exist and include more sophisticated processes like silicon-on-insulator and advanced device structures. Thus, the limitation of the physical properties (low bandgap) of silicon can be stretched by working around the high intrinsic carrier concentration at higher temperatures and the critical electric field of 300kV/cm.

In contrast, silicon carbide – especially the 4H-SiC polytype – exhibits a wide bandgap of 3.2kV which does not come with the temperature and electric field restrictions of silicon. Here, new applications can be enabled at temperatures beyond 300°C and at high electric fields for power semiconductor devices. However, without the economy driving technology development similar to Si CMIS, SiC processing technology is still at an early stage. In this paper distinct challenges for SiC CMOS device fabrication using planar technology are described and first solutions for manufacturing SiC CMOS circuits are presented.

Activation of dopants at 1700°C prevents the implementation of self-aligned channel technology routinely used in silicon. Therefore, an alternative process flow has to be implemented. This paper presents a standard implementation sequence based on process modules to realize CMOS based circuits and high voltage devices.

Manufacturing of SiC devices in planar technology utilizes doping by ion implantation. Besides activation at higher temperatures than in silicon, channeling of ions occurs to a higher degree in SiC. Moreover, fabrication of implanted regions with aluminum is hampered by defects which constitute compensation sites in 4H-SiC. In an attempt to understand these effects, TCAD modelling has been implemented to help predict the outcome of a selected manufacturing technology. This way, the desired channel length can be achieved and short channel effects can be avoided.

Results of device modelling and comparison to electrical measurements will be presented. Additionally, the present status of advanced device manufacturing using charge-compensation patterns for RESURF LDMOS transistors is discussed in detail.

The manufacturing technology used for integrated SiC CMOS circuits is also applicable to sensors. Results of SiC UV sensors and SiC temperature sensors are also shown.

The paper concludes with an outlook towards future device performance and application examples.

Keywords: *SiC CMOS, integrated circuits, integrated sensors, SiC LDMOS, RESURF*

References

[1] Weisse J., Hauck M., Sledziewski T., Tschiesche M., Krieger M., Bauer A.J., Mitlehner H., Frey L., Erlbacher T., “Analysis of Compensation Effects in Aluminum-Implanted 4H-SiC Devices”, Material Science Forum 924 (2018) 184-187

[2] Matthus C.D., Bauer A.J., Frey L., Erlbacher T., “Wavelength-selective 4H-SiC UV-sensor array”, Mat. Sci.

Semicond. Proc. 90 (2019) 205-211
[3] Matthus C.D., DiBenedetto L., Kocher M., Bauer A.J., Licciardo G.D., Rubino A., Erlbacher T., “Feasibility of 4H-SiC p-i-n Diode for Sensitive Temperature Measurements Between 20.5K and 802K”, IEEE Sensors Journal 19 (2019) 2871-2878

Biography

Tobias Erlbacher received the Diploma in Electrical Engineering (Microelectronics) from the University of Erlangen-Nuremberg in 2004, and his Ph.D. degree in 2008. Since 2009 he is with the Fraunhofer Institute of Integrated Systems and Device Technology IISB in Erlangen, where he is heading the “Devices” Group. He has authored and coauthored over 70 papers in scientific journals and contributed to 7 patent families.