Process and design optimization of SiC MOSFET for low on-state resistance

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Abstract

Due to outstanding material parameters, silicon carbide (SiC) power devices offer much better electrical and thermal parameters than comparable silicon power devices in the same blocking voltage range. One of the key parameters of the power MOSFET is its on-state resistance, RDS(on) which has to be small, in order to obtain small power loss in a forward current conduction mode. In this work we present how process and design of SiC MOSFET can be optimized for the low on-state resistance. We distinguish different components of the total on-state resistance, which are the substrate and drift resistance; the channel, accumulation and JFET resistance; the source and contact resistance; and we show how each of these components has been minimized for our devices by the recent process developments. In addition to the process optimization, we discuss various ways to improve the SiC MOSFET design, which in general lead to larger cell integration and result in the lower on-state resistance of the device. These are for example a usage of a square elementary cell and an application of the short-channel technology. Results presented in this work are the experimental and simulation data collected during the academic, industrial and joint-research projects at Fraunhofer IISB.

Part of this research was supported by GRDC Program through the National Research Foundation (NRF) funded by the MSIT of Korea (NRF-2017K1A4A3013716).

Keywords: *Silicon Carbide, Semiconductor, 4H-SiC, MOSFET*